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Karen Vertz	(Depositor's name)
<i>Karen Vertz</i>	(Signature)
4-22-04	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,514	07/29/2003	Craig T. Salling	TI-32206.1	6919

TITLE OF INVENTION: METHOD TO INCREASE SUBSTRATE POTENTIAL IN MOS TRANSISTORS USED IN ESD PROTECTION CIRCUITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	07/16/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOGANS, DAVID L	2813	438-527000

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1 W. James Brady, III2 Frederick J. Telecky, Jr.

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4-22-04

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OMB 0651-0033

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PAGE 2/2 * RCVD AT 4/22/2004 10:05:12 AM [Eastern Daylight Time] * SVR:USPTO-EFXXF-2/0 * DNIS:7464000 * CSID:972 917 4417 * DURATION (mm-ss):01-16



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant Craig T. Salling, et al.

Docket Number: TI-32206.1

Serial No.: 10/629,514

Art Unit: 2813

Filed: 07/29/03

Examiner: David L. Hogans

For: Method to Increase Substrate Potential in MOS Transistors
Used in ESD Protection Circuits

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NAME OF INVENTOR(S): Craig T. Salling, et al.	
TITLE OF INVENTION: Method to Increase Substrate Potential in MOS Transistors Used in ESD Protection Circuits	
TI FILE NO.: TI-32206.1	DEPOSIT ACCT. NO.: 20-0668
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RECEIPT DATE & SERIAL NO.: Serial No.: 10/629,514 Filing Date: 07/29/03	

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